In the Claims:

Please amend claim 6 and add new claims 8 and 9 to appear as indicated in the following listing of claims, which replaces all prior versions.

1. (Original) A Phase Locked Loop comprising a frequency detector including an unbalanced quadricorrelator, the quadricorrelator comprising a frequency detector including double edge clocked bi-stable circuits coupled to a first multiplexer and to a second multiplexer being controlled by a signal having a same bitrate as the incoming signal, and a phase detector controlled by a first signal pair provided by the first multiplexer and by a second signal pair provided by the second multiplexer.

2. (Original) A Phase Locked Loop as claimed in claim 1, wherein the frequency detector comprises a first pair of double edge clocked bi-stable circuits coupled to the first multiplexer, and a second pair of double edge clocked bi-stable circuits coupled to the second multiplexer, which first and second pairs are supplied by mutually quadrature phase shifted signals respectively to provide the first signal pair and the second signal pair indicative for a phase difference between the incoming signal and mutually quadrature phase shifted signals.

3. (Original) A Phase Locked Loop as claimed in claim 1, wherein the phase detector comprises a D flip-flop receiving the first signal pair and being clocked by the second signal pair, the second signal pair being inputted to respective gates of a first transistors pair for determining a state ON or OFF of a current through said first transistors pair.

4. (Original) A Phase Locked Loop as claimed in claim 3, wherein current through the first transistor pair biases a second transistor pair, the second transistor pair receiving the first signal pair and generating an output signal indicative for a frequency error between the incoming data signal and Clock signals.

5. (Original) A Phase Locked Loop as claimed in claim 2, wherein the mutually

quadrature phase shifted signals are generated by a voltage controlled oscillator.

6. (Currently amended) A Phase Locked Loop as claimed in 5, wherein a frequency error signal produced by the quadricorrelator ~~the error signal~~ is inputted to a coarse control input of the voltage controlled oscillator via a first charge pump coupled to a first low-pass filter coupled to an adder.

7. (Original) A Phase Locked Loop as claimed in claim 6, wherein a fine control input is controlled by a signal provided by a phase detector coupled to a second charge pump coupled to second low-pass filter.

8. (New) A Phase Locked Loop comprising:

a voltage controlled oscillator having a coarse control input and a fine control input;

a quadricorrelator generating a frequency error signal inputted to the coarse control input of the voltage controlled oscillator via a first charge pump coupled to a first low-pass filter coupled to an adder, the quadricorrelator including

a frequency detector including a first pair of double edge clocked bi-stable circuits coupled to a first multiplexer and a second pair of double edge clocked bi-stable circuits coupled to a second multiplexer to provide a second signal pair, the first and second pairs of bi-stable circuits being supplied by mutually quadrature phase shifted signals generated by the voltage controlled oscillator, the first and second multiplexers being controlled by a signal having a same bitrate as the incoming signal and respectively providing a first signal pair and a second signal pair indicative for a phase difference between an incoming signal and mutually quadrature phase shifted signals;

a phase detector controlled by the first signal pair and the second signal pair, the phase detector including a D flip-flop receiving the first signal pair and being clocked by the second signal pair, the second signal pair being inputted to respective gates of a first transistors pair for determining a state ON or OFF of a current through said first transistors pair; and

a second phase detector generating a phase error inputted to the fine control input of the voltage controlled oscillator via a second charge pump coupled to a second low-pass filter.

9. (New) The Phase Locked Loop of claim 8, wherein the phase error is further inputted to the coarse control input of the voltage controlled oscillator via the second charge pump coupled to a third low-pass filter couple to the adder.